AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter (where underlining "_" denotes additions and strikethrough "-" denotes deletions).

Claims:

1. (Currently Amended) A method for reducing CPU loading in a software receiver for a packet based communications system comprising the steps of:

measuring the current CPU load by measuring an interrupt latency;

determining whether the CPU load has exceeded a predetermined threshold;

responsive to determining that the CPU has exceeded a predetermined threshold, entering a power save mode by setting a Power Save (PS) bit in a frame control word, thereby signaling the communications system transmitter to inhibit packet transmission and packet reception;

monitoring the CPU load while the transmitter is inhibited;

determining that the CPU load has fallen below a predetermined threshold; and

signaling the communications system transmitter to begin transmitting packets once the CPU load has fallen below the predetermined threshold, wherein the signaling clears the PS bit.

2. (Original) A method as in claim 1, wherein the measurement of CPU loading is made by an operating system background task.

3. (Canceled)

4. (Previously Presented) A method as in claim 1, wherein the transmitter signaling is performed during the power save mode.

5. (Original) A method as in claim 1, in which the communications system is wireless.

6. (Original) A method as in claim 1, in which the communications system is IEEE 802.11 wireless local area network (WLAN).

7. (Original) A method as in claim 1, in which the communication system is Bluetooth.

8. (Original) A method as in claim 1, in which the communications system is IEEE 802.15 wireless personal area network (PAN).

9.-14. (Canceled).

15. (Currently Amended) ~~A computer-readable medium encoded with~~ An apparatus for reducing CPU loading in a software receiver for a packet based communications system comprising:

a processor configured with digital logic configured to:

measure the current CPU load by measuring the response time of the CPU to a request for processor time;

determine whether the CPU load has exceeded a predetermined threshold;

responsive to determining that the CPU has exceeded a predetermined threshold, enter a power save mode by setting a Power Save (PS) bit in a frame control word, thereby signaling the communications system transmitter to inhibit packet transmission and packet reception;

monitor the CPU load while the transmitter is inhibited;

determine whether the CPU load has fallen below a predetermined threshold; and

signal the communications system transmitter to begin transmitting packets once the CPU load has fallen below the predetermined threshold, wherein the signaling clears the PS bit.

16. (Currently Amended) The ~~computer-readable medium~~ apparatus of claim 15, wherein the measurement of CPU loading is a background task.

17. (Currently Amended) The ~~computer-readable medium~~ apparatus of claim 15, wherein the CPU load measurement is based on the response time of a host CPU to a request for interrupt.

18. (Currently Amended) The ~~computer-readable medium~~ apparatus of claim 15, wherein the transmitter signaling is performed during the power save mode.

19. (Currently Amended) The ~~computer-readable medium~~ apparatus of claim 15, wherein the communications system is wireless.

20. (Currently Amended) The ~~computer-readable medium~~ apparatus of claim 15, wherein the communications system is at least one of: an IEEE 802.11 wireless local area network (WLAN); a Bluetooth system; and an IEEE 802.15 wireless personal area network (PAN).

21. (Currently Amended) A system for reducing CPU loading in a software receiver for a packet based communications system comprising a ~~computer-readable medium~~ processing means comprising:

means for measuring the current CPU load by measuring an interrupt latency;

means for determining whether the CPU load has exceeded a predetermined threshold;

means for, responsive to determining that the CPU has exceeded a predetermined threshold, entering a power save mode by setting a Power Save (PS) bit in a frame control word, thereby signaling the communications system transmitter to inhibit packet transmission and packet reception;

means for monitoring the CPU load while the transmitter is inhibited;

means for determining that the CPU load has fallen below a predetermined threshold; and

means for signaling the communications system transmitter to begin transmitting packets once the CPU load has fallen below the predetermined threshold, wherein the signaling clears the PS bit.

22. (Previously Presented) The system of claim 21, wherein the measurement of CPU loading is made as a background task.

23. (Canceled)

24. (Previously Presented) The system of claim 21, wherein the transmitter signaling is performed during the power save mode.

25. (Previously Presented) The system of claim 21, wherein the communications system is wireless.

26. (Previously Presented) The system of claim 21, wherein the communications system is at least one of: an IEEE 802.11 wireless local area network (WLAN); a Bluetooth system; and an IEEE 802.15 wireless personal area network (PAN).